WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a dielectric layer having an upper surface over a conductive feature;

forming an opening in the dielectric layer exposing an upper surface of the conductive feature;

forming a silicon carbide layer, having a silicon surface, lining the opening;

depositing a barrier layer on the silicon surface of the silicon carbide layer; and

filling the opening with copper (Cu) or a Cu alloy.

2. The method according to claim 1, comprising:

forming the dielectric layer by depositing a first dielectric layer, depositing a middle etch stop layer on the first dielectric layer and depositing a second dielectric layer on the middle etch stop layer; and

forming the opening as a dual damascene opening comprising a lower via hole section in the first dielectric layer and upper trench section in the second dielectric layer.

3. The method according to claim 2, comprising forming the silicon carbide layer having the silicon surface lining the opening by:

depositing a layer of silicon carbide having a silicon surface over the upper surface of the second dielectric layer, lining the opening and on the upper surface of the conductive feature; and

removing the silicon carbide layer from over the second dielectric layer and from on the upper surface of the conductive feature, leaving the silicon carbide layer having the silicon surface lining the trench section and via hole section.

4. The method according to claim 2, comprising forming the silicon carbide layer with the silicon surface at a thickness of 30 Å to 90 Å.

5. The method according to claim 4, comprising forming the silicon carbide liner with the silicon surface, such that the silicon surface has a thickness of 10 Å to 20 Å.

6. The method according to claim 2, comprising forming the silicon carbide layer with the silicon surface by sequentially:

introducing a wafer having the dielectric layer with the dual damascene opening therein into a chamber;

introducing trimethyl silane (TMS) and helium (He) into the chamber for a period of time sufficient to stabilize the TMS flow rate at 100 to 200 sccm and to stabilize the He flow rate at 100 to 1,000 sccm;

introducing ammonia (NH_3) to establish a flow rate of 200 to 600 sccm;

applying an RF power of 240 to 360 watts to initiate plasma enhanced chemical vapor deposition (PECVD) of a layer silicon carbide;

discontinuing the introduction of TMS, He and NH_3 into the chamber;

reducing the RF power to 120 to 180 watts; and

introducing silane (SiH_4) into the chamber to deposit a layer of silicon on the silicon carbide layer to form the silicon surface.

7. The method according to claim 6, comprising introducing TMS and He into the chamber for about 5 to about 35 seconds before introducing NH_3 into the chamber.

8. The method according to claim 6, comprising:

depositing the layer of silicon carbide at a thickness of 20 Å to 70 Å; and

depositing the layer of silicon at a thickness of 10 Å to 20 Å to form the silicon surface.

9. The method according to claim 6, comprising introducing SiH_4 into the chamber to establish a flow rate of 50 to 200 sccm.

10. The method according to claim 2, wherein each of the first and second dielectric layers comprises a dielectric material having a dielectric constant (k) no greater than 3.9.

11. The method according to claim 10, where each of the first and second dielectric layers comprises a dielectric material with a porosity of about 10% to about 20%.

12. A semiconductor device comprising:

a dielectric layer formed over a conductive feature having an upper surface;

an opening in the dielectric layer over the upper surface of the conductive features;

a silicon carbide layer having a silicon surface region lining the opening;

a diffusion barrier layer on the silicon surface region of the silicon carbide layer and in contact with the upper surface of the conductive feature; and

copper (Cu) or Cu alloy filling the opening.

13. The semiconductor device according to claim 12, wherein:

the dielectric layer comprises a first dielectric layer, a middle etch stop layer on the first dielectric layer and a second dielectric on the middle etch stop layer; and

the opening is a dual damascene opening comprising a lower via hole second in the first dielectric layer and an upper trench section in the second dielectric layer.

14. The semiconductor device according to claim 13, wherein each of the first and second dielectric layers comprises a dielectric material having a dielectric constant (k) no greater than 3.9.

15. The semiconductor device according to claim 14, wherein each of the first and second dielectric layers comprises a dielectric material having a porosity of 10% to 20%.

16. The semiconductor device according to claim 13, wherein the thickness of the silicon carbide layer with the silicon surface region is 30 Å to 90 Å.

17. The semiconductor device according to claim 16, wherein the silicon surface region has a thickness of 10 Å to 20 Å.

18. The semiconductor device according to claim 13, wherein the barrier layer comprises tantalum, tantalum nitride, or a composite comprising a layer of tantalum nitride on the silicon carbide layer and a layer of tantalum on the layer of tantalum nitride.

19. The semiconductor device according to claim 14, wherein the silicon carbide layer having the silicon surface region has a combined thickness of 30 Å to 90 Å.

20. The semiconductor device according to claim 19, wherein the silicon-rich surface region has a thickness of 10 Å to 20 Å.